REMARKS

Claims 1-13 and 21-27 are pending in this application. Claims 14-20 are canceled herein. Claims 1, 2, 4, 7, 8, and 11-13 have been amended and claims 21-27 have been added herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

Claims 1-13 were rejected under 35 U.S.C. 112 first paragraph as failing to comply with the enablement requirement. Applicant respectfully disagrees, but does acknowledges that portions of the specification (between about paragraph 30-41 as originally presented) do require a careful and thoughtful reading. However, it is also submitted that paragraphs from about paragraph 42 through 73 are clear and clarify paragraphs 30-41. Paragraphs 30-41 also clearly support and enable the claims. Therefore, although a few clarification changes have been added to the specification paragraphs between paragraphs 42 and 73, more extensive clarifications are included (with respect to paragraphs 30-41) to correct and clarify the idiomatic English resulting from the translations of the specification from German to English. However, it is further submitted that the changes are all nothing more than clarifications and no changes are made that are not obvious clarifications or that are not clearly supported by the original specification, drawings, or claims.

Claims 1-13 were rejected under 35 U.S.C. 112, second paragraph as being indefinite. However, a new claim 21 has been added and all of the original dependent claims now depend from new claim 21. Further, claim 1 has been amended and six new dependent claims have been added to depend therefrom. Therefore, it is respectfully submitted that all of the claims are now definite, do properly define the invention, and are allowable.

In addition, the following paragraphs may further help understanding of the invention.

The present invention relates to a method of increasing the size of main structures such as trenches, formed at a selected depth of a semiconductor substrate. In particular, the invention relates to a method of etching deep trenches for trench storage capacitors in a monocrystalline silicon substrate, wherein the storage capacitors are arranged alternately with selection transistors in a checkered fashion. According to the invention, the deep trenches are expanded below the selected depth in the semiconductor substrate to increase the capacitor size and the resisting capacitance. In order to optimally expand the size of the deep trenches and thus to optimally underetch the selection transistor structures, advantage is taken of the fact that the etching rate for standard etching processes depends on the orientation of the crystal faces in the semiconductor substrate.

When the checkered pattern is aligned in parallel at the surface, with a crystal face having a first orientation, is compared with a crystal face having a second orientation rotated 45°, the semiconductor substrate is etched at a first rate. In comparison, side walls remaining in the extended portion of the deep trench after an expanding etching process are formed by the crystal faces having the second orientation. Since the side walls of the non-extended upper portion of the deep trench are formed of crystal faces having the first orientation, the result is a configuration of deep trenches whose lower portions each are rotated through 45° with respect to the upper portion, so that utilization of the space in the depth is optimized in the case of a checkered pattern.

However, when the checkered pattern is aligned in parallel with the crystal faces having the second orientation, the usable surface is restricted to the region of the deep trench fields,

since both in the upper and in the lower region the side walls of the deep trench are formed of crystal faces having the second and same orientation.

According to the method under the present invention, an orthogonal surface pattern is preferably aligned in accordance with the <100> crystal orientation of the monocrystalline semiconductor substrate.

Applicant respectfully submits three replacement drawing sheets indicating that FIGs. 2, 4A-4C, and 7A are prior art.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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